REMARKS

This RESPONSE is submitted in response to the Office Action mailed October 5, 2004, and is believed to be fully responsive thereto for the following reasons.

Responsive to paragraphs 1 and 3-5, the claims have been amended appropriately to obviate the noted objection and rejection.

Reconsideration is respectfully requested of the rejections of:

Claims 1-7 and 9-23 under 35 U.S.C. 102(b) as being anticipated by Botula, et al. (U.S. Serial No. 6,429,489 B1), in paragraph 7 of the Office Action;

Claim 8 under 35 U.S.C. 103(a) as being unpatentable over Botula, et al. (U.S. Serial No. 6,429,489 B1), in view of Weiss (U.S. Patent No. 6,600,356 B1), in paragraph 17 of the Office Action;

Claims 1-7 and 9-23 under the judicially created doctrine of double patenting over Claims 1-10 of U.S. Patent No. 6,429,489 B1, in paragraph 20 of the Office Action; and

Claim 8 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 1 of U.S. Patent No. 6,429,489 B1 in view of Weiss (U.S. Patent No. 6,600,356 B1), in paragraph 21 of the Office Action.

The present invention is substantially different from Botula, et al., which is acknowledged prior art in Figure 1 of the subject patent application.

Please note the explanation on page 4 with respect to Botula, et al.

"The prior art as developed to date has been constrained by the Johnson Limit as discussed below in providing a low trigger voltage condition for ESD protection circuits,

particularly on-chip ESD protection circuits for CMOS and BiCMOS chips for RF applications."

The Botula, et al. circuit is described on page 7 of the subject patent application.

"Figure 1 illustrates an exemplary circuit of a prior art SiGe ESD power clamp wherein a first stage low breakdown transistor device serves as a trigger for a second stage high breakdown clamp transistor device. The first stage trigger transistor has a resistor R_{bias} in series therewith between power supplies V_{DD} and V_{SS}, and the second stage clamp transistor has a resistor $R_{ballast}$ in series therewith between the power supplies VDD and VSS. The circuit of Figure 1 is a common emitter circuit with SiGe or SiGeC devices having floating bases, wherein the devices closely approximate the Johnson Limit curve.

Figure 1 illustrates an exemplary Darlington configured bipolar power clamp circuit with a sub-native trigger voltage. For this configuration to be suitable as an ESD power clamp, we can take advantage of the inverse relationship between the BV_{CEO} and the f_T of the device. For a power clamp, the clamp device must have a high breakdown voltage in order to address the functional potential between the V_{CC} power supply and ground potential. This power clamp requires a f_T above the ESD pulse frequency to discharge the current effectively. For the trigger device, a low breakdown voltage device is needed in order to initiate base current into the clamp device at an early enough voltage."

Botula, et al. discloses a SiGe ESD power clamp in a Darlington ytpe configuration, Figure 3, where a trigger transistor 202 has a collector-to-emitter break-down voltage (BVCEO) that is lower than that of the clamping transistor 206, and a frequency cutoff that is higher than that of the clamping device. (Abstract)

Note that the Botula circuit (also Figure 1 of this patent application) comprises a trigger transistor in a collector to emitter breakdown voltage (BVCEO) configuration. This is a reverse biased collector to emitter configuration.

Contrast the circuits of Figures 3 and 4 of the present invention wherein the trigger device is a forward biased pn junction diode device (not a transistor).

Note also that independent Claim 1 (and independent Claims 11, 17 and 21) specifies a forward biased trigger device and a clamp transistor.

See also the description of the trigger device on pages 8 and 9 of this patent application.

"The ESD trigger device is preferably a forward biased junction element in Si or SiGe or SiGeC and comprises the following general categories of junction elements:

1. CMOS, BiCMOS and RF CMOS diodes, including Si LOCOS defined pn diodes, Si shallow trench isolation defined pn diodes with a medium or deep trenches, polysilicon gate defined pn diodes, all of which can be in Si, SiGe or SiGeC technologies, in either P well or N well, and all of which can include features of subcollectors, trench isolation, with medium or deep trench structures;

2. bipolar devices, including Si, SiGe or SiGeC diode configured bipolar npn or pnp transistors as two element components, Si, SiGe or SiGeC varactors, usually configured base-collector;

3. Schottky diodes in either Si, SiGe or SiGeC;

4. MOSFETs, in either P channel or N channel, including low voltage trigger MOSFETs, gate modulated pseudo-zero V_T MOSFETs, depletion MOSFETs and dynamic threshold MOSFET diodes."

Please note that all of the above devices are single pn junction devices. Category 2 mentions npn or pnp transistors but they are "diode configured...as two element components", which means that only 1 pn junction of the transistor is being used, and the device is not being used as a complete npn or pnp transistor.

The present invention has several major distinguishing features over Botula

1) A first major distinction is that the present invention provides a trigger device which is not a transistor as disclosed in Botula. The present invention utilizes a "trigger device' and a "clamp transistor", which includes only a single transistor, whereas Botula contains at least 2 transistors, one trigger transistor and one clamp transistor.

2) A second major distinction is that the present invention avoids usage of a trigger element in a BVCEO configuration as disclosed in Botula. The present invention uses a "forward biased" trigger device, whereas Botula utilizes a trigger transistor device in a reverse-biased collector-to-emitter configuration.

3) A third major distinction is that in the present invention the trigger voltage can be lower than the BVCEO of the fastest transistor in the technology, which is not possible in Botula. The present invention responds to a trigger voltage below the Johnson Limit of the fastest transistor in the technology, whereas Botula discloses a trigger network whose trigger voltage is associated with the Johnson Limit relationship.

In view of the above explanations, Claim 1 has been amended to more clearly distinguish over Botula, and distinguishes over Botula in the first and third paragraphs as follows. The added claim limitation in the first paragraph is directly supported in the specification at the end of paragraph [0019].

"a forward biased trigger device fabricated in a given technology, wherein the trigger device is forward biased by a voltage to conduct in a non-breakdown, non-rectifying mode of operation;

a clamp transistor coupled to the trigger device so that activation of the trigger device activates the clamp transistor, the clamp transistor having a cutoff frequency which determines its Johnson Limit breakdown voltage;

the trigger device being fabricated in the given technology and having a trigger activation voltage above which the trigger device activates the clamp transistor, with the trigger activation voltage being below the Johnson Limit breakdown voltage of the highest frequency device fabricated in the given technology."

Weiss

Weiss has a plurality of elements, base resistance, and the transistors QDE1, and QED2. In contrast, the present invention does not utilize a plurality of forward biased elements. In the present invention, the total number of elements should be such that it is lower than the BVCEO of the output transistor. Adding more elements as in Weiss leads to a higher not lower trigger condition. The present invention does not require QDE1, and QDE2 due to an increase in the turn-on voltage as well as an increase in the "on" resistance. This impacts the on-resistance and ESD robustness of the network. The present invention can contain low voltage elements, instead of the addition of these elements as in Weiss.

This application is now believed to be in condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,

William C. Roch
Registration No.: 24,972

Scully, Scott, Murphy & Presser
400 Garden City Plaza, Suite 300
Garden City, New York 11530
(516) 742-4343

WCR:gc